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-	3489	(optimiz\$5 or optimis\$5) same (data near3 access\$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/17 16:51
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-	13	(optimiz\$5 or optimis\$5) adj (data near3 access\$3) and ((data or pattern) near2 usage)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/10 10:28
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-	237	code adj analysis and (access\$3 or usage)	USPAT	2004/08/10 11:44
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-	3500	(optimiz\$5 or optimis\$5) same (data near3 access\$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/17 16:51
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Pages:539 - 546
[\[Abstract\]](#) [\[PDF Full-Text \(688 KB\)\]](#) **IEEE CNF**
2 Partial indexing for nonuniform data distributions in relational DBM*Sartori, C.; Scalas, M.R.;*Knowledge and Data Engineering, IEEE Transactions on , Volume: 6 , Issue: 3 , June 1994
Pages:420 - 429
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3 Hybrid FDD/SDD-WCDMA system architecture: joint power control : space diversity for demand access channels*Wong, W.W.S.; Sousa, E.S.;*Communications, 2000. ICC 2000. 2000 IEEE International Conference on , Volume: 1 , 18-22 June 2000
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1 [How to solve the current memory access and data transfer bottlenecks: at the processor architecture or at the compiler level](#)

Francky Catthoor, Nikil D. Dutt, Christoforos E. Kozyrakis

January 2000 **Proceedings of the conference on Design, automation and test in Europe**

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Chye Lin Chee; Hongjun Lu; Hong Tang; Ramamoorthy, C.V.;

Knowledge and Data Engineering, IEEE Transactions on , Volume: 10 , Issue: 5 , Sept.-Oct. 1998

Pages:824 - 838

[\[Abstract\]](#) [\[PDF Full-Text \(600 KB\)\]](#) **IEEE JNL**

Data and memory optimization techniques for embedded systems

P. R. Panda, F. Catthoor, N. D. Dutt, K. Danckaert, E. Brockmeyer, C. Kulkarni, A. Vandercappelle, P. G. Kjeldsberg

April 2001 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 6 Issue 2

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We present a survey of the state-of-the-art techniques used in performing data and memory-related optimizations in embedded systems. The optimizations are targeted directly or indirectly at the memory subsystem, and impact one or more out of three important cost metrics: area, performance, and power dissipation of the resulting implementation. We first examine architecture-independent optimizations in the form of code transformations. We next cover a broad spectrum of optimizati ...

Keywords: DRAM, SRAM, address generation, allocation, architecture exploration, code transformation, data cache, data optimization, high-level synthesis, memory architecture customization, memory power dissipation, register file, size estimation, survey